CLAIMS

What is claimed is:

1. A method, comprising:

a) measuring a skew between a data signal and a clock signal at a receiving end of a serial link; and

b) adjusting a phase relationship between said data signal and said clock signal to reduce said skew.

2. The method of claim 1 wherein said adjusting of said phase relationship occurs at a transmitting end of said serial link.

3. The method of claim 1 further comprising receiving said measured skew at a skew adjustment unit and determining said phase relationship before said adjusting a phase relationship.

4. The method of claim 1 further comprising programming said phase relationship into a semiconductor chip.

5. The method of claim 1 wherein said adjusting a phase relationship further comprises imposing a delay on at least one of said signals.

6. The method of claim 5 wherein said adjusting a phase relationship further comprises imposing a delay on both of said signals.

7. The method of claim 1 wherein said adjusting a phase relationship further comprises adjusting a phase offset between a pair of phasors associated with a pair of phase interpolators, a first of said phasors used to derive a second clock

signal that times the transmission of said data signal, a second of said phasors used to derive said clock signal.

8. An apparatus, comprising:

a) a transmitting unit coupled to a receiving unit by a serial link, said serial link configured to transport a clock signal and a data signal;

b) a skew measurement unit coupled to said serial link such that said coupling of said skew measurement unit to said serial link is closer to said receiving unit than said transmitting unit; and

c) a skew adjustment unit coupled to said skew adjustment and said transmitting unit.

9. The apparatus of claim 8 further comprising a programmable delay unit within said transmitting unit, said programmable delay unit coupled to said skew adjustment unit, said programmable delay unit output corresponding to one of said signals.

10. The apparatus of claim 8 further comprising a second programmable delay unit within said transmitting unit, said second programmable delay unit coupled to said skew adjustment unit, said programmable delay unit output corresponding to another of said signals.

11. The apparatus of claim 9 wherein said programmable delay unit further comprises a cascade of inverters.

12. The apparatus of claim 11 wherein each of said inverters within said cascade of inverters has an adjustable propagation delay.

13. The apparatus of claim 8 wherein transmission of said data signal is timed according to a phase interpolator output.

14. The apparatus of claim 8 wherein clock signal is derived from a phase interpolator output.

15. The apparatus of claim 14 wherein said phase interpolator further comprises a skew control input that adjusts a phasor phase offset, said skew control input coupled to said skew adjustment unit.

16. The apparatus of claim 8 wherein said skew adjustment unit further comprises a CPU.

17. An apparatus, comprising:

a) a network interface coupled to a transmitting unit;

b) a receiving unit coupled to said transmitting unit by a serial link, said serial link configured to transport a clock signal and a data signal;

c) a skew measurement unit coupled to said serial link such that said coupling of said skew measurement unit to said serial link is closer to said receiving unit than said transmitting unit; and

d) a skew adjustment unit coupled to said skew adjustment and said transmitting unit.

18. The apparatus of claim 17 wherein transmission of said data signal is timed according to a phase interpolator output.

19. The apparatus of claim 17 wherein clock signal is derived from a phase interpolator output.

20. The apparatus of claim 19 wherein said phase interpolator further comprises a skew control input that adjusts a phasor phase offset, said skew control input coupled to said skew adjustment unit.

21. The apparatus of claim 17 wherein said skew adjustment unit further comprises a CPU.

22. The apparatus of claim 17 wherein said transmitting unit further comprises a parallel to serial converter that crafts said data signal, said parallel to serial converter receiving parallel data from said network interface.

23. The apparatus of claim 17 wherein said network interface corresponds to a physical layer.

24. The apparatus of claim 17 wherein said network interface corresponds to a media access control layer.